SystemVerilog For Design: A Guide to Using SystemVerilog for Hardware Design and Modeling

Stuart Sutherland, Simon Davidmann, Peter Flake

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SystemVerilog is a rich set of extensions to the IEEE 1364-2001 Verilog Hardware Description Language (Verilog HDL). These extensions address two major aspects of HDL based design. First, modeling very large designs with concise, accurate, and intuitive code. Second, writing high-level test programs to efficiently and effectively verify these large designs.

This book, **SystemVerilog for Design**, addresses the first aspect of the SystemVerilog extensions to Verilog. Important modeling features are presented, such as two-state data types, enumerated types, user-defined types, structures, unions, and interfaces. Emphasis is placed on the proper usage of these enhancements for simulation and synthesis. A companion to this book, **SystemVerilog for Verification**, covers the second aspect of SystemVerilog.

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